IN THE CLAIMS:

1. (Currently Amended) A method for testing an integrated circuit, comprising:

providing a wafer having multiple die that are separated by a singulation area and each containing the integrated circuit;

providing a visual functional indicator for ~~each of~~ some or all of the multiple die, the visual functional indicator indicating functionality of multiple circuit modules of an associated die and is contained on or adjacent to the associated die;

providing test circuitry on each of the some or all of the multiple die, the test circuitry being dedicated specifically for testing an associated one ~~each~~ of the some or all of the multiple die that have a visual functional indicator in response to receiving a test enable signal at an input pad thereof;

powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;

performing predetermined tests with the test circuitry for the some or all of the multiple die;

outputting a test result to the visual functional indicator for each of the some or all of the multiple die; ~~and~~

using the test result to create a visual indication on or adjacent the ~~wafer~~ some or all of the multiple die with each visual functional indicator corresponding to the test result; and

recording the visual functional indicator for each of the some or all of the multiple die on or after a fixed predetermined time after receiving the test enable signal.

2. (Currently Amended) The method of claim 1 further comprising:

physically locating ~~the~~ a single visual functional indicator within each of the some or all of the multiple die.

3. (Original) The method of claim 1 further comprising:

physically locating the visual functional indicator external to the some or all of the multiple die and within a scribe area of the wafer.

4. (Currently Amended) The method of claim 1 further comprising:

implementing the visual functional indicator as a light ~~emitting diode (LED)~~ indicating device that provides a predetermined code value indicative of the test result.

5. (Currently Amended) The method of claim 1 further comprising:

providing a single visual functional indicator for each of the some or all of the multiple die and sequentially testing multiple modules of each of the some or all of the multiple die and sequentially indicating a test result for the multiple modules with the single visual indicator ~~repeating the predetermined tests to test the some or all of the multiple die under a plurality of differing operating conditions to determine whether the some or all of the multiple die are functional within a range of operating conditions~~.

6. (Currently Amended) The method of claim 1 further comprising:

~~providing multiple visual indicators on each of the some or all of the die, each of the multiple visual indicators indicating functional operation of a separate predetermined portion of a predetermined one of the some or all of the multiple die~~ resetting the test circuitry to an initial state in response to powering up the wafer.

7. (Currently Amended) A ~~The~~ method for testing an integrated circuit ~~of claim 1 further~~ comprising:

providing a wafer having multiple die that are separated by a singulation area;

providing a visual functional indicator for each of some or all of the multiple die;

providing test circuitry for each of the some or all of the multiple die that have a visual functional indicator;

powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;

performing predetermined tests with the test circuitry for the some or all of the multiple die;

outputting a test result to the visual functional indicator for the some or all of the multiple die;

using the test result to create a visual indication on the wafer with each visual functional indicator corresponding to the test result; and

implementing the visual functional indicator as a binary coded decimal (BCD) light emitting diode (LED) that asserts a predetermined decimal upon passing a corresponding predetermined functional test.

8. (Original) The method of claim 1 further comprising:

singulating the multiple die and segregating functional die of the multiple die from non-functional die of the multiple die based upon the visual indication.

9. (Currently Amended) A ~~The~~ method ~~of claim 1 further~~ for testing an integrated circuit comprising:

providing a wafer having multiple die that are separated by a singulation area;

providing a visual functional indicator for each of some or all of the multiple die;

providing test circuitry for each of the some or all of the multiple die that have a visual functional indicator;

powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;

performing predetermined tests with the test circuitry for the some or all of the multiple die;

outputting a test result to the visual functional indicator for the some or all of the multiple die;

using the test result to create a visual indication on the wafer with each visual functional indicator corresponding to the test result; and

recording the visual indication with either a camera or a high resolution imager to form a data base that is used by a singulation tool to singulate the multiple die and segregate the multiple die based on the visual indication.

Claims 10-19. (Previously Canceled).

20. (Currently Amended) A method for testing an integrated circuit, comprising:

providing a wafer having multiple die that are separated by a singulation area;

providing a visual functional indicator for multiple functional modules of each of the multiple die thereby providing a plurality of visual indicators distributed across the wafer;

providing ~~test circuitry~~ a dedicated built-in self-test (BIST) circuit for each of the multiple die;

powering up the wafer to electrically activate the multiple die and initiate operation of the ~~test circuitry~~ built-in self-test (BIST) circuit;

performing predetermined tests with the test circuitry for each of the multiple die;

outputting a test result to the visual functional indicator for each of the multiple die; and

using the test result to create a visual indication on the wafer with each visual functional indicator corresponding to the test result and providing a predetermined value indicative of the test result.

21. (Original) The method of claim 20 further comprising:
using a portion of the plurality of visual indicators for both a test mode of operation and a normal functional mode of operation.

22. (Original) The method of claim 20 further comprising:
positioning each respective visual functional indicator within a corresponding respective one of the multiple die.

23. (Original) The method of claim 20 further comprising:
implementing each visual functional indicator with a light emitting diode (LED).

24. (Currently Amended) A method for testing an integrated circuit, comprising:
providing a wafer having multiple die;
providing a visual functional indicator for each of a plurality of the multiple die;
~~providing~~ coupling dedicated test circuitry ~~for~~ to the visual functional indicator in each of the multiple die that have a visual functional indicator;
powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;
enabling the test circuitry with an enable signal applied to an input of each of the plurality of the multiple die;
performing predetermined tests with the test circuitry for each of the plurality of the multiple die; ~~and~~
outputting a test result to each visual functional indicator to visually indicate which die of the multiple die passed the predetermined tests and which die failed the predetermined tests; and
using imaging means to inspect each visual functional indicator and record test results.

25. (Original) The method of claim 24 further comprising:

physically locating each functional indicator within a scribe area of the wafer.

26. (Currently Amended) A ~~The~~ method ~~of claim 24 further~~ for testing an integrated circuit comprising:

providing a wafer having multiple die;

providing a visual functional indicator for each of the multiple die;

providing test circuitry for each of the multiple die that have a visual functional indicator;

powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;

performing predetermined tests with the test circuitry for the multiple die;

outputting a test result to each visual functional indicator to visually indicate which die of the multiple die passed the predetermined tests and which die failed the predetermined tests; and

recording each visual functional indicator with either a camera or a high resolution imager to form a data base that is used by a singulation tool to singulate the multiple die and segregate the multiple die based on each visual functional indicator.